



Innovation in research and engineering education:  
key factors for global competitiveness  
*Innovación en investigación y educación en ingeniería:  
factores claves para la competitividad global*

# UNDERSTANDING THE PROPERTIES OF RF-MOSFETS USING THE SMITH CHART

**Roberto Murphy Arteaga, Reydezel Torres Torres, Fabián Zárate Rincón**

**Instituto Nacional de Astrofísica, Óptica y Electrónica  
Tonantzintla, Puebla, México**

## **Abstract**

The advancement of technology has made wireless communications ubiquitous, and thus they represent a major field of study nowadays. The demand for engineers able to design circuits and systems to operate in the microwave regime is increasing every day, and universities and graduate schools have to form them in the best possible way, giving them the abilities and competences needed to succeed in this field.

One of the motors for the fast development and evolution of wireless communications circuits and systems is the Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET or MOS Transistor). The MOS transistor is the basis for CMOS (Complementary MOS) circuits, which employs transistors of positive (P-Channel) and negative (N-Channel) charge carriers to achieve very low power consumption without degrading the required figures-of-merit of the circuit. Additionally, CMOS circuits can be fabricated at very low cost, which makes them attractive for a vast array of commercial applications.

Consequently, research on the high-frequency properties and behavior of MOS transistors is ongoing, and has become a very important component of engineering curricula, both at the undergrad and graduate levels.

The purpose of this paper is to present an innovative approach to reading S-Parameters from Smith Charts that allows students to directly interpret the properties of the device under test (DUT). With this approach, they can easily judge several of the most important transistor parameters, such as matching conditions, open or short circuit non-idealities, input impedance and its capacitive component, the value of Source and Drain series resistances, leakage currents, channel resistance, substrate losses, and intrinsic capacitances, among others.

**Keywords:** MOS transistor; high-frequency; Smith chart

## **Resumen**

*El avance de la tecnología se ha traducido en comunicaciones inalámbricas ubicuas, por lo que ahora representan un campo de estudio de mucha importancia. La demanda de ingenieros capaces de diseñar circuitos y sistemas para operación en el rango de las microondas aumenta día con día, y las universidades y escuelas de graduados los tienen que formar de la mejor manera posible, impartiendo las habilidades y competencias necesarias para ser exitosos en el campo.*

*Uno de los motores responsables del rápido desarrollo y evolución de los circuitos y sistemas para comunicaciones inalámbricas es el transistor de efecto de campo Metal-Óxido-Semiconductor (MOSFET o Transistor MOS, por sus siglas en inglés). El transistor MOS es la base de los circuitos CMOS (MOS Complementario), que usan portadores positivos (Canal P) y negativos para lograr un muy bajo consumo de potencia sin degradar las figuras de mérito del circuito. Además, los circuitos CMOS se pueden fabricar a muy bajo costo, lo que los hace atractivos para una gama amplia de aplicaciones comerciales.*

*Es por esto que se realizan muchos esfuerzos de investigación sobre las propiedades y respuesta del transistor MOS en el rango de altas frecuencias, temas que se han incorporado importantemente en el currículo, tanto de pre-grado como de postgrado.*

*El objetivo de este artículo es presentar un enfoque innovador para la lectura de Parámetros S directamente de la Gráfica Smith, que le permite a los estudiantes deducir rápidamente las propiedades del dispositivo bajo prueba (DBP). Con este enfoque, pueden fácilmente juzgar varios de los parámetros del transistor, como son el acoplamiento, no-idealidades debidas a cortos y circuitos abiertos, la impedancia de entrada y su componente capacitiva, el valor de las resistencias de Fuente y Drenaje, corrientes de fuga, la resistencia del canal, pérdidas por el substrato, y las capacitancias intrínsecas, entre otros.*

**Palabras Clave:** transistor MOS; altas frecuencias; carta de Smith

## **1. Introduction**

Due to the ever-more widespread use of CMOS circuitry in modern wireless communication systems, a thorough knowledge of the MOS transistor has become mandatory. In order to design and simulate a circuit using these transistors, the devices have to be characterized in the laboratory. And even though the MOS transistor is a generic device, with small variations from vendor to vendor, each process produces a unique device that has to be measured and characterized independently in order to obtain reliable and scalable models to accurately simulate a circuit. These models are obtained as a result of intensive data correlation with experimental measurements collected from carefully designed test-chips containing numerous devices.

Nowadays, the most widely used techniques to characterize high-speed devices such as MOS transistors involve the measurement of “Scattering Parameters”, or “S-Parameters” for short, which relate reflected and transmitted power waves incident on the device at each terminal. In fact, these parameters are the only ones that can be reliably measured at high frequencies since their measurement does not require a “short circuit” or an “open circuit” condition at any of the terminals or ports. S-Parameters can be measured using either coaxial or coplanar probes connected to the device’s ports. In the case of measurements in the gigahertz range on on-chip devices, the most popular measurement technique employs probe tips to directly contact

the chip's probing pads in order to avoid the relatively large parasitics introduced when using coaxial connectors.

Nevertheless, even in this case the characterization process can be time consuming, since the experimental set-up has to be calibrated up to the probe-tips before performing measurements on the DUT (Device Under Test) (see, for instance, Rytting (1998) and Stenarson et al. (2008)). An example of a typical set-up is shown in Figure 1.

Once the calibration has been verified, S-Parameter measurements of the DUT are taken, and displayed in different formats on the screen of the Vector Network Analyzer (VNA) in use. At this point, the user can get qualitative information on the behavior of the DUT; to extract accurate quantitative figures, the data have to be converted to other sets of small-signal parameters, such as impedance ( $Z$ ), admittance ( $Y$ ), inverse transmission (ABCD), or hybrid (H). This is generally done after all measurements have been performed and electronically stored. Several examples of these techniques can be found in the references (Álvarez et al. (2011); Torres et al. (2003), (2004), (2005); Zárate et al. (2012)).

If the qualitative behavior is not adequate, however, the quantitative data might be meaningless, and the measurement process has to be repeated. In order to obtain trustworthy data from the initial measurement, the user has to be able to read the Smith Chart provided by the VNA, and judge if the DUT's response is what it is expected. Thus, a quick interpretation of these data is mandatory.

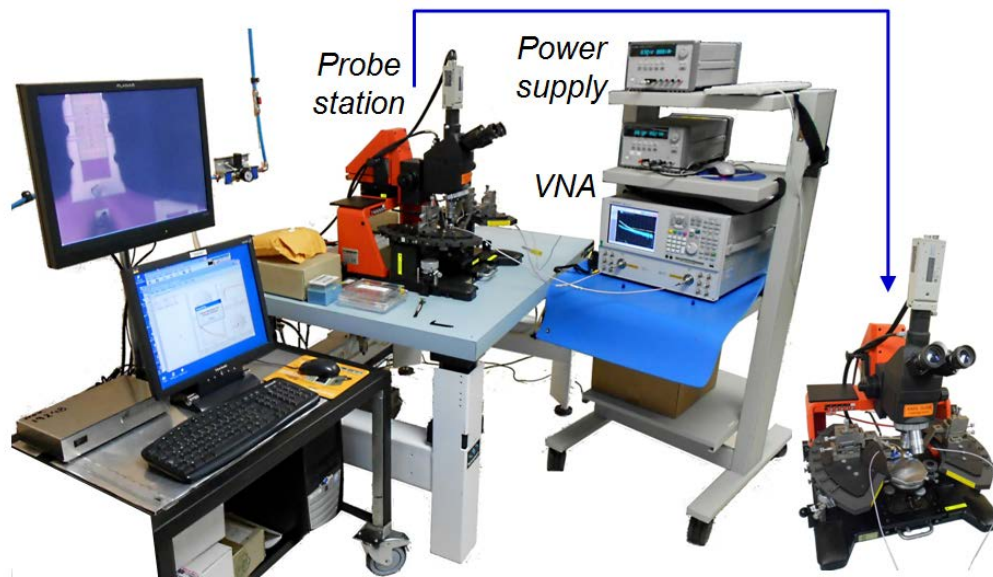


Figure 1. A typical set-up to measure high frequency S Parameters.

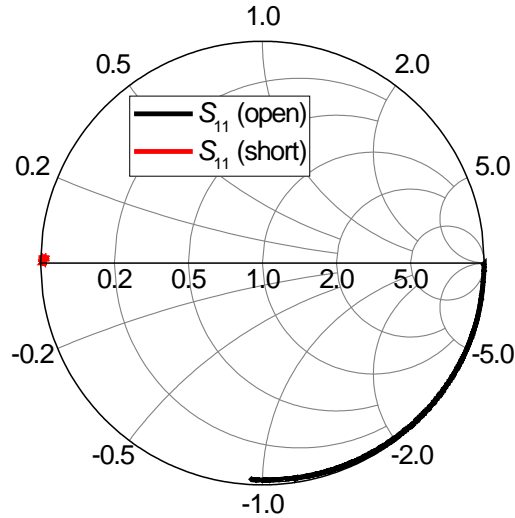


Figure 2. Smith Chart for on-wafer Short and Open structures.

For instance, Figure 2 shows the Smith Chart corresponding to the measurement of dummy structures built on the same chip (these are used for the de-embedding process, which will not be addressed in this paper, but the interested reader can refer to Ferndahl et al. (2008) and Kang et al. (2009)). An ideal “short” presents a reflection coefficient of  $-1$ , which is a dot on the left-hand side of the x-axis. An ideal “open” presents a reflection coefficient of  $+1$ , or a point on the right-hand side of the x-axis on the Smith Chart.

In Figure 2 we can note that the dummy short approaches the ideal behavior, whereas the open is not perfect. The Smith Chart, however, indicates that the reflection coefficient is close to  $+1$  in all the frequency range, showing a capacitive response.

## 2. Characterization of the MOST

In order to fully characterize the transistor, different bias schemes are employed. This is due to the fact that depending on the operating region, some components dominate over others, and fewer components have to be determined in each step. Generally, the first step measures the transistor in the “off” state; the second considers the transistor in strong inversion but without any flow of current ( $V_{ds}=0$ ); and the last step measures the transistor in any of the “on” states. These steps are detailed hereafter, with their corresponding S-Parameter Smith Charts.

### 2.a. MOSFET in the “off” state (cold condition)

Figure 3 shows the equivalent circuit for the device under the “cold condition”, that is, when all applied voltages are equal to zero.

Under these bias conditions, the components associated with the extrinsic part of the transistor can be determined, since the transistor is in the “off” state and the intrinsic components do not play a part in the response. A quick glance of the Smith Chart, shown in Figure 4, provides the basic information on input and output impedances, when measured in the 10MHz to 20GHz range (the trace is always clockwise). The input impedance is due to the Gate resistance and the oxide capacitance, whereas  $S_{22}$  gives information on the

parasitic capacitances due to Gate overlap and junction capacitances, which constitute the main components of the output impedance.

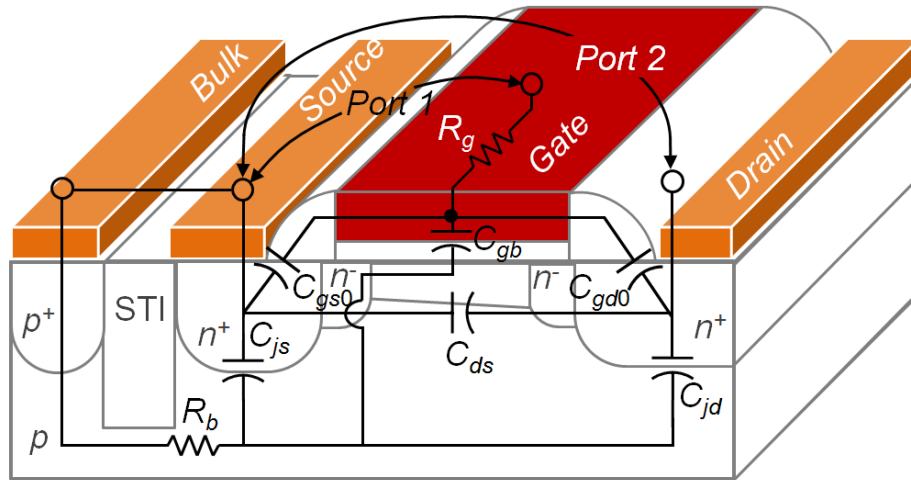


Figure 3. RF-MOSFET at  $V_{gs}=V_{ds}=V_{bs}=0V$ .

As can be seen,  $S_{11}$  traces a curve following the  $r=0.2$  curve, which upon de-normalizing can be interpreted as an effective input resistance of about 100  $\Omega$ . The output impedance is initially higher, following the  $r=0.5$  circle, but tends to lower values as the frequency increases. The transmission coefficients,  $S_{12}$  and  $S_{21}$ , trace the same curve, since in this case the device is can be considered as symmetrical.

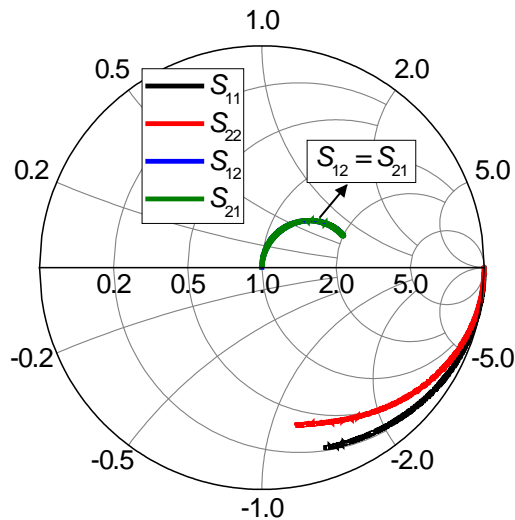


Figure 4. S-Parameters for the MOST under the “cold condition” bias.

**2.b. MOSFET in strong inversion**

Figure 5 shows the transistor biased in strong inversion, but with  $V_{ds}=0$ , while Figure 6 presents the corresponding S-Parameter Smith Chart. Under this bias condition, the channel is inverted, providing

conduction from Drain to Source, but since the potential difference between these terminals is zero, there is no current flow.  $S_{11}$  still shows a capacitive behavior, the curve being traced under the  $r=0.2$  circle.  $S_{22}$ , however, is purely resistive, and basically consists of the combination of Source and Drain resistances, in series with the channel resistance, which constitute the output impedance, close to the  $r=0.1$  circle or equivalent to  $50 \Omega$  which indicates that the transistor output is adequately matched. Since no current is flowing ( $V_{DS}=0$ ), the inversion layer is uniform, and the transistor can be considered symmetric, and thus  $S_{12}=S_{21}$  as in the previous case.

The user can then use these four sets of data to globally judge the performance of the DUT. The capacitive input impedance is expected, since the transistor's Gate is isolated from the channel region by a dielectric layer. It includes the parasitic overlap capacitances. The output impedance is due mainly to resistive components, and thus it should appear as a dot on the horizontal axis for this bias condition. Its value can be inferred, and compared to the designed output impedance. Finally, the fact that the transmission coefficients are the same implies that the measurement was correctly performed; process variations in geometry or conductivity are taken into account either way the transistor is measured, and they do not affect the symmetry of these coefficients.

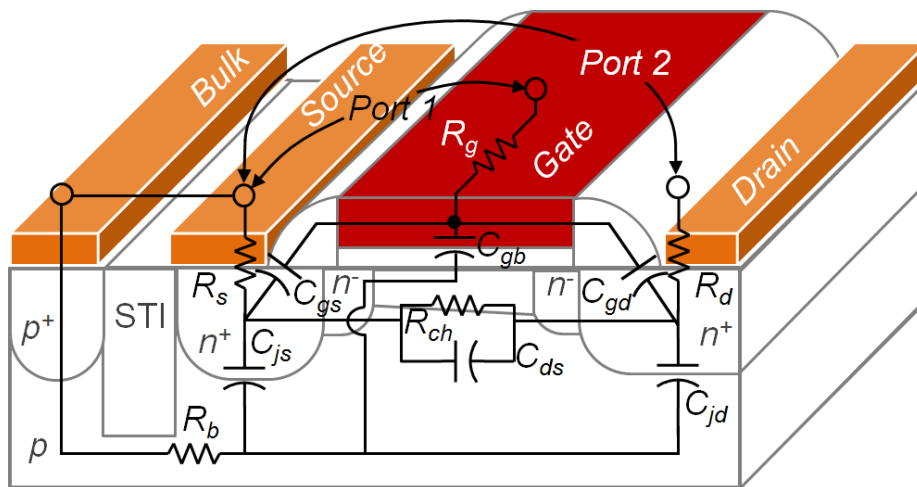


Figure 5. RF-MOSFET in strong inversion at  $V_{GS}=0.6V$  and  $V_{DS}=V_{BS}=0V$ .

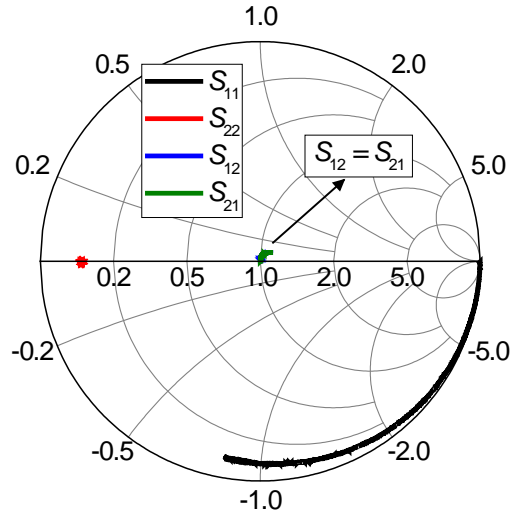


Figure 6. Smith Chart showing the S-Parameters for the MOST biased in strong inversion.

**2.c. MOSFET in the “on” state (active region)**

The device is then biased in the active region;  $V_{gs} > V_{th}$  and  $V_{ds} > 0$ . Under these bias conditions, the channel is formed, and there is a current flow from Drain to Source. The shape of the inversion layer will no longer be uniform, and the device will perform as an amplifier if correctly designed. Figure 7 shows the equivalent circuit for the device, while the S-Parameters for the device operating in the saturation region are shown in Figure 8.

As can be expected from the previous discussion, the input impedance, given by  $S_{11}$ , is still mostly capacitive, but the reflection coefficient deviates from +1; it traces a curve almost following the  $r=0.2$  circle, but deviates to lower resistance values as the frequency increases.  $S_{22}$  is now purely capacitive for the measurement frequency range, but tending to the upper plane of the chart as frequency increases. This is indicative of a higher current flow through the associated substrate components such as  $C_{jd}$ .

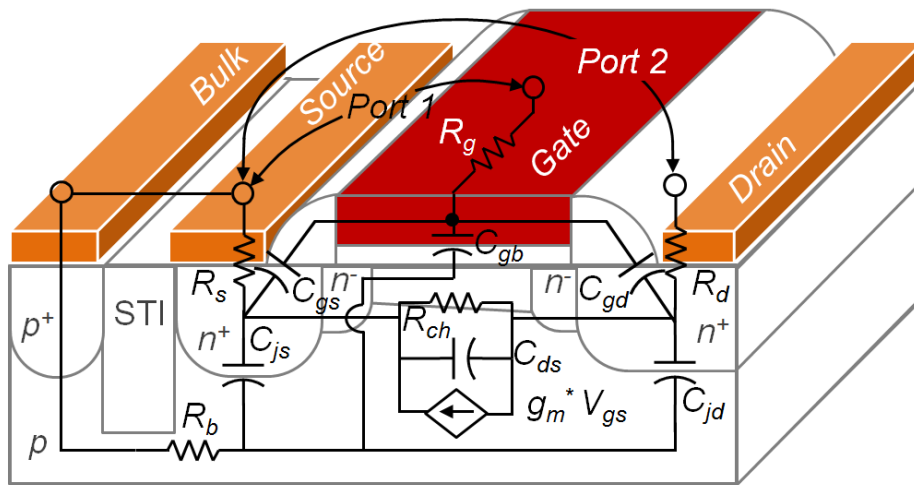


Figure 7. RF-MOSFET in the active region at  $V_{gs}=0.6V$ ,  $V_{ds}=0.7V$  y  $V_{bs}=0V$ .

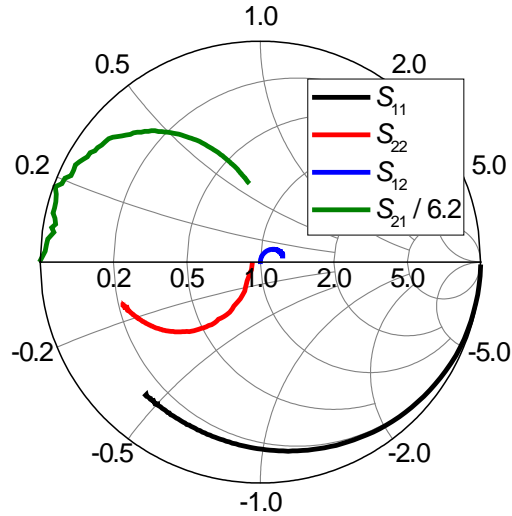


Figure 8. S-Parameter Smith Chart for the device operating in the saturation region.

The transmission coefficients are now radically different; on the one hand,  $S_{12}$  still presents a very small value, whereas  $S_{21}$  (normalized on the graph in Figure 8) is quite large. This is indicative of the transistor gain, and it clearly means that in this operating regime the transistor is not symmetrical; the inverse gain is much less than the forward gain.

### 3. Conclusions

A quick interpretation of the S-Parameter Smith Chart gives the student an important amount of qualitative information regarding the behavior of a DUT as a function of frequency. Even though quantitative results are needed, these are obtained after processing and analyzing the data, which is generally done after the measurement session. Since it is highly recommendable to calibrate the equipment for each session, it is of fundamental importance that the data shown on the VNA screen are reasonable, and that a quick visual inspection can guarantee that this is so. If the user can trust the data as seen directly from the VNA screen, it is very likely that the quantitative information obtained after processing the measurement results will be trustworthy and the need for another measurement session will be avoided. The experience with our graduate students has been truly satisfying; their comments are positive in the sense that they believe this interpretation has helped substantially to make efficient use of their laboratory time. Based on these comments, we recommend that the method be used at the undergraduate level also. Much more information can be obtained from the Smith Chart, but due to space limitations, only a broad scope has been presented here.

### 4. References

- Álvarez, G.A., Torres, R., Murphy, R. (2011). Using S-parameter Measurements to Determine the Threshold Voltage, Gain Factor, and Mobility Degradation Factor for Microwave Bulk-MOSFETs. *Microelectronics Reliability*, Vol. 51, No. 2, pp. 342-349.
- Ferndahl, M., Fager, C., Andersson K., Linnér, P., Vickes, H.O., Zirath, H. (2008). A General Statistical Equivalent-Circuit-Based De-Embedding Procedure for High Frequency Measurements. *IEEE Transactions on Microwave Theory and Techniques*, Vol. 56, No. 12, pp. 2692-2700.



- Kang, I.M., Jung, S.J., Choi, T.H., Jung, J.H., Chung, C., Kim, H.S., Oh, H., Lee, H.W., Jo, G., Kim, Y.K., Kim, H.G., Choi, K.M. (2009). Five-Step (Pad-Pad Short-Pad Open-Short-Open) De-Embedding Method and Its Verification. IEEE Electron Device Letters, Vol. 30, No. 4, pp. 398-400.
- Rytting, D. (1998). Network Analyzer Error Models and Calibration Methods. Agilent Technologies White Paper, 1998, pp. 1-43.
- Stenarson, J., Yhland, K., (2008). An Overview of VNA Calibration and Uncertainty Evaluation Techniques. Proceedings of the 2008 German Microwave Conference, Hamburg, Germany, pp. 428-431.
- Torres, R., Murphy, R., Decoutere, S. (2003). MOSFET Gate Resistance Determination. Electronics Letters, Vol. 39, No. 2, pp. 248-250.
- Torres, R., Murphy, R. Torres, A. (2004). An Improved Substrate-Loss Model to Determine MOSFET Drain, Source and Substrate Elements. Microwave and Optical Technology Letters, Vol. 43, No. 2, pp. 126-130.
- Torres, R. Murphy, R. (2005). Enabling a Compact Model to Simulate the RF Behavior of MOSFETs in SPICE. International Journal of RF and Microwave Computer-Aided Engineering, Vol. 15, No. 3, pp. 255-263.
- Zárate, F., Álvarez, G.A., Torres, R., Murphy, R. (2012). Extraction Methodology of the Substrate Parasitic Network of an RF-MOSFET with Separate Substrate DC Connection. Proceedings of the XVIII International IBERCHIP Workshop, Playa del Carmen, México, pp. 155-159.

#### About the authors:

- **Roberto Murphy** is a senior researcher with the Electronics Department of INAOE, where he has worked on the high-frequency characterization of semiconductor devices and passive components since 1988. [rmurphy@inaoep.mx](mailto:rmurphy@inaoep.mx)
- **Reydezel Torres** is a senior researcher with the Electronics Department of INAOE, specializing in the high-frequency characterization of devices and PCB components. [reydezel@inaoep.mx](mailto:reydezel@inaoep.mx)
- **Fabián Zárate** is a Ph.D. student in the Electronics Department of the INAOE, working on high-frequency characterization of MOS transistors. [fabian\\_zar@inaoep.mx](mailto:fabian_zar@inaoep.mx)

---

Los puntos de vista expresados en este artículo no reflejan necesariamente la opinión de la Asociación Colombiana de Facultades de Ingeniería y de la International Federation of Engineering Education Societies

Copyright © 2013 Asociación Colombiana de Facultades de Ingeniería (ACOFI), International Federation of Engineering Education Societies (IFEES)